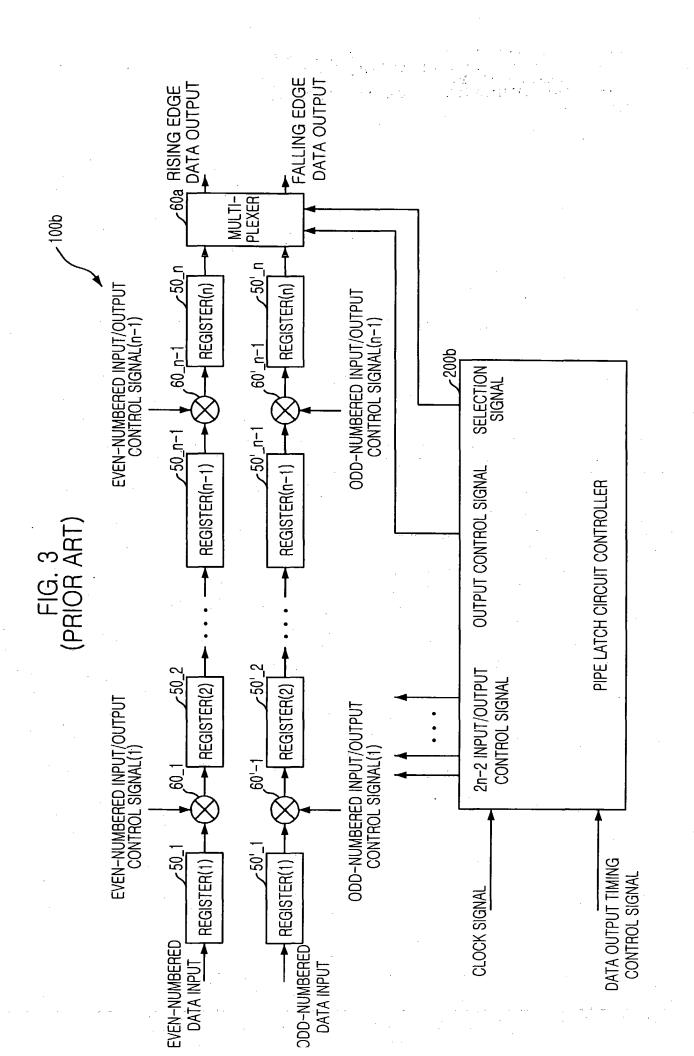
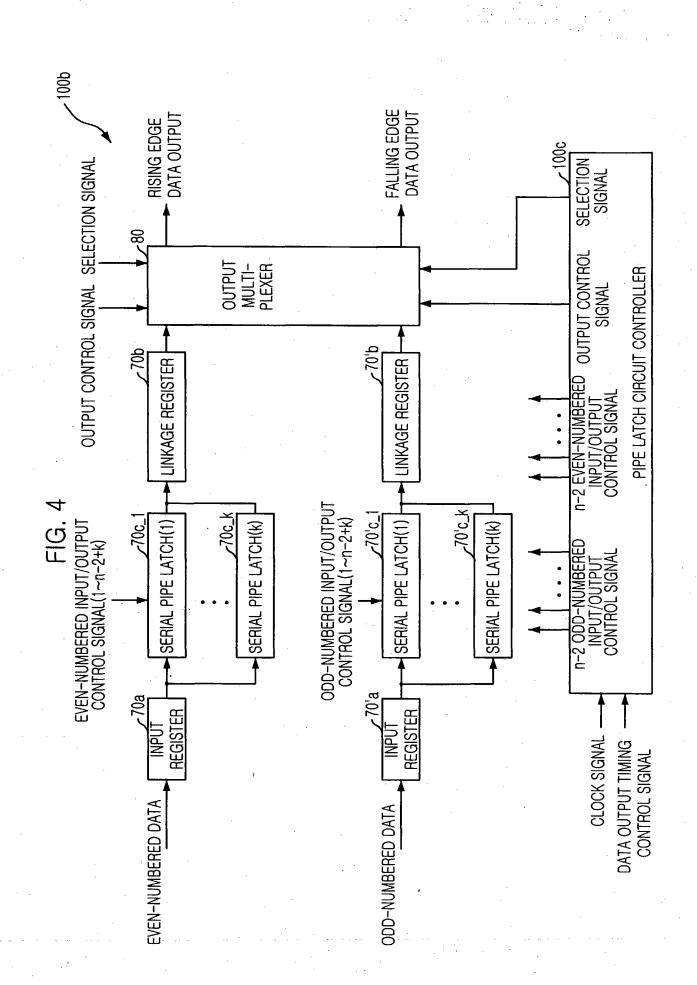
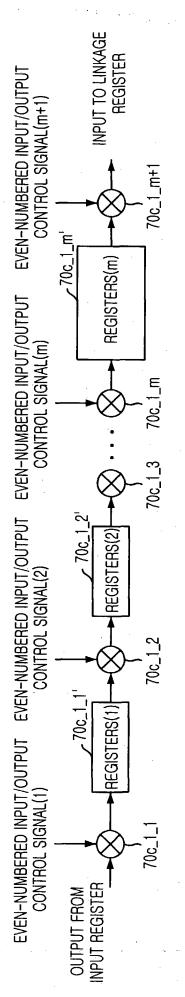


FIG. 2B (PRIOR ART)

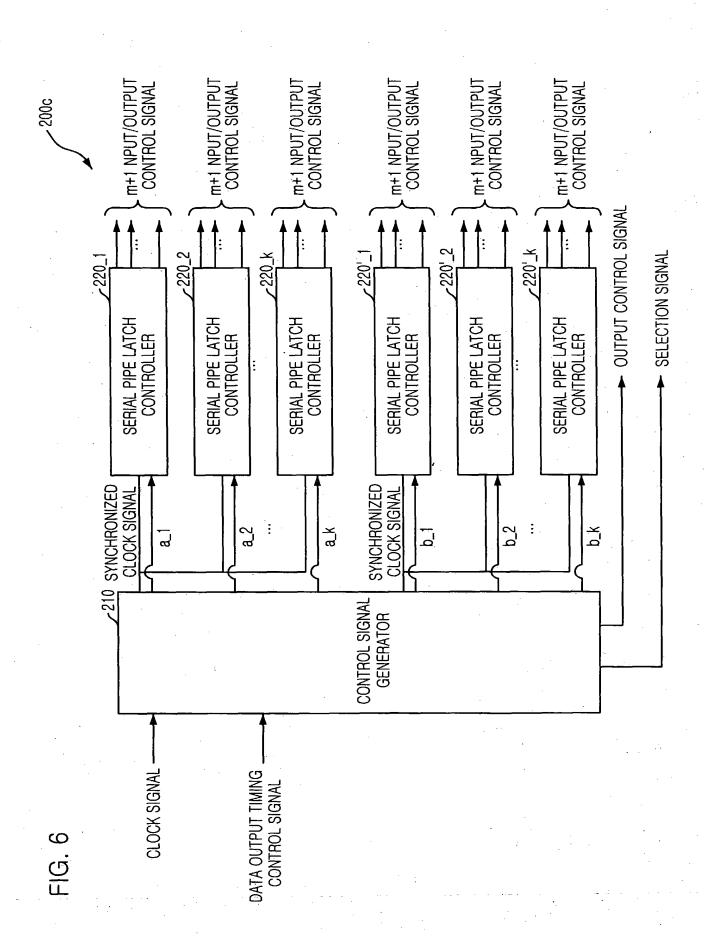


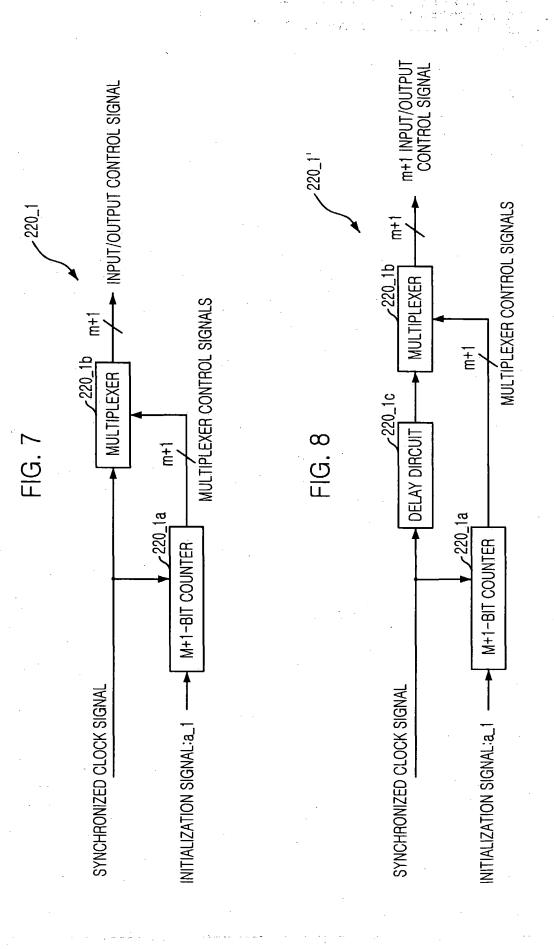




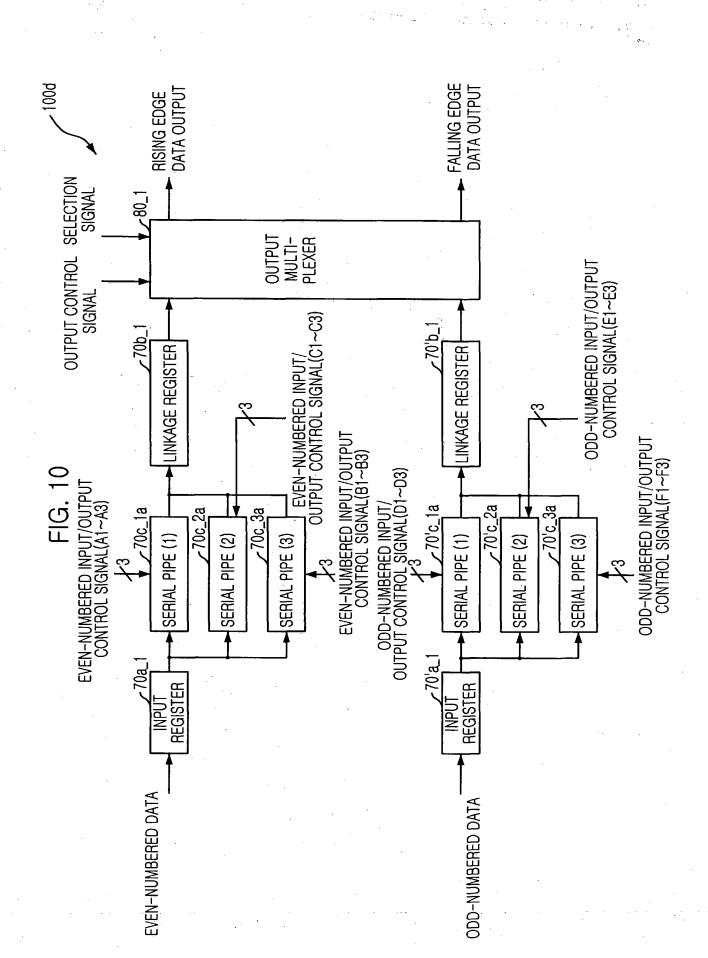


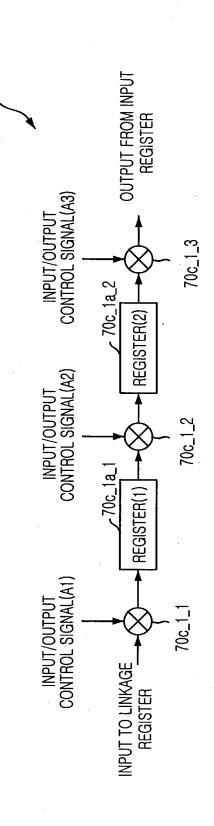
m=(n-2)/ k (n: REGISTERS (k: NUMBER OF SERIAL PIPE LATCHES





:	CONVENTIONAL PIPE LATCHES		PIPE LATCHES ACCORDING
	PARALLEL	SERIAL	TO THE PRESENT INVENTION
REGISTER	2n(16)	2n(16)	2n(16)
MULTIPLEXER	n(8)	1(1)	1(1)
PATH CIRCUIT	4n(32)	2n-2(14)	(2n-4)+2k(18)
TOTAL	7n(56)	4n-1(31)	(4n-3)+2k(35)
CONTROL SIGNAL	4n(40)	2n-2(16)	(2n-4)+2k(18)





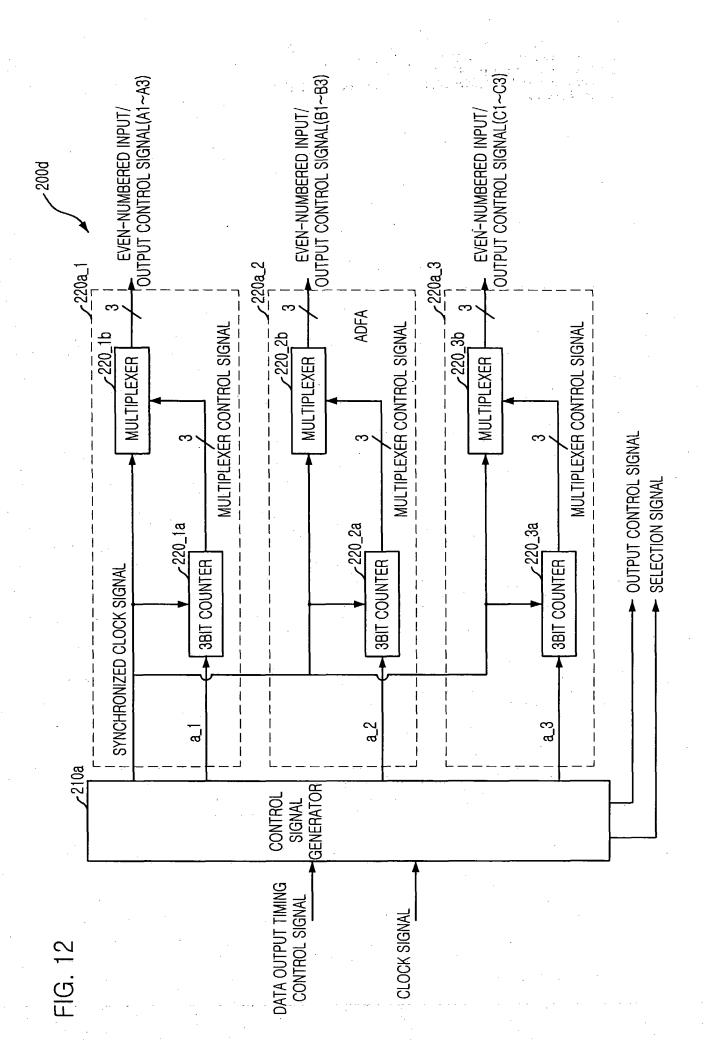


FIG. 13

220a_1

FIG. 14

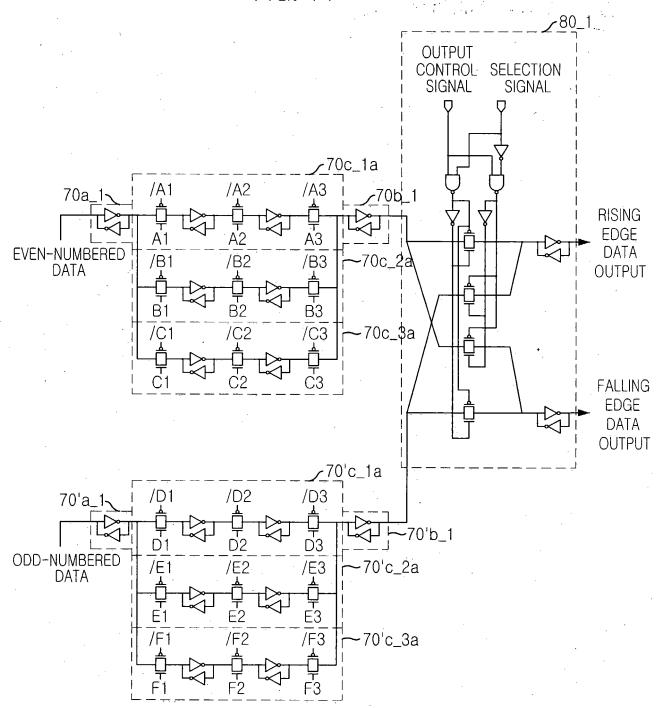


FIG. 15

